OB233F

High Performance Current Mode PWM Power Switch

GENERAL DESCRIPTION

OB233F combines a dedicated current mode PWM controller with a high voltage power MOSFET. It is optimized for high performance, low standby power, and cost effective off-line flyback converter applications.

OB233F offers complete protection coverage with automatic recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), over voltage protection and VDD under voltage lockout (UVLO). Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique together with soft switching control at the totem pole gate drive output.

The tone energy at below 20KHZ is minimized in the design and audio noise is eliminated during operation.

OB233F is offered in DIP7 package.

APPLICATIONS

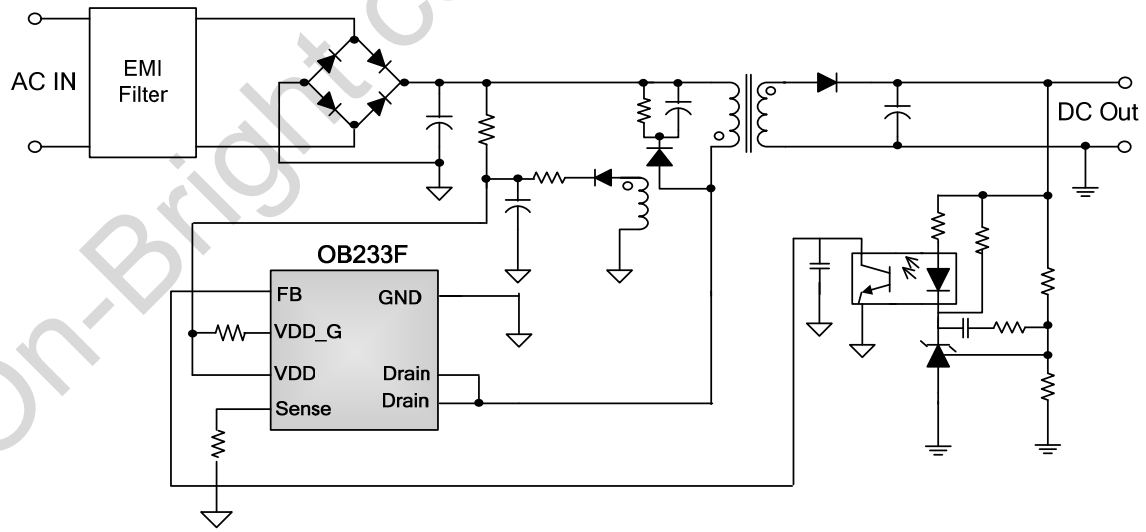
Offline AC/DC flyback converter for

- AC/DC adapter
- PDA power supplies
- Digital cameras and camcorder adapter
- VCR, SVR, STB, DVD&DVCD Player SMPS
- Set-top box power
- Auxiliary power supply for PC and Server
- Open-frame SMPS

FEATURES

- Standby power lower than 100mW at universal AC input
- Power on soft start reducing Power MOSFET Vds stress
- Frequency shuffling for EMI
- Extended burst mode control for improved efficiency and minimum standby power design
- Audio noise free operation
- Fixed 65KHZ (typical) switching frequency
- Internal synchronized slope compensation
- Low VDD startup current and low operating current
- Leading edge blanking on current sense input
- Comprehensive protection coverage
  - o VDD under voltage lockout with hysteresis (UVLO)
  - o Over temperature protection (OTP) with auto- recovery
  - o On-Bright proprietary line input compensated
  - o Cycle-by-Cycle over-current threshold setting for constant output power limiting over universal input voltage range.
  - o Accurate overload protection (OLP).
  - o Over voltage protection(OVP)
  - o Secondary rectifier short protection

TYPICAL APPLICATION



Output Power Table

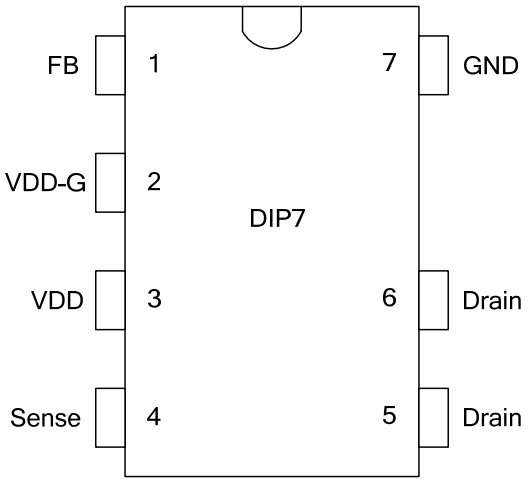
Product	230VAC±15% Adapter[1]	85-265VAC Adapter[1]
OB233F	23W	18W

Notes: 1. Maximum practical continuous power in an adapter design with sufficient drain pattern as a heat sink, at 40℃ ambient.

GENERAL INFORMATION

Pin Configuration

The OB233F is offered in DIP7 package as shown below.



Ordering Information

Part Number	Description
OB233FSP	DIP7, Pb-free

Package Dissipation Rating

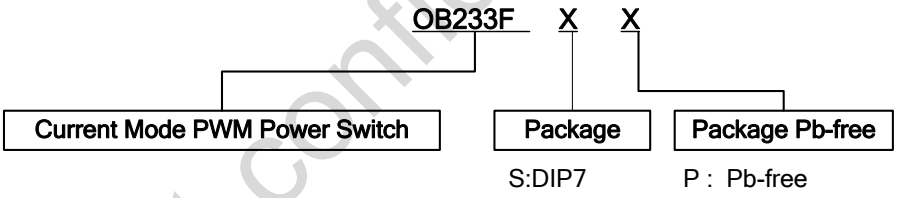
Package	RθJA (℃/W)
DIP7	75

Note: Drain Pin Connected to 100mm^2 PCB copper clad.

Absolute Maximum Ratings

Parameter	Value
Drain voltage (off state)	-0.3V to BVdss
VDD voltage	-0.3V to 30 V
VDD-G input voltage	-0.3V to 30 V
FB input voltage	-0.3 to 7V
Sense input voltage	-0.3 to 7V
Min/Max operating junction temperature T_J	-40 to 150℃
Min/Max storage temperature T_{stg}	-55 to 150℃
Lead temperature (soldering, 10secs)	260℃

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



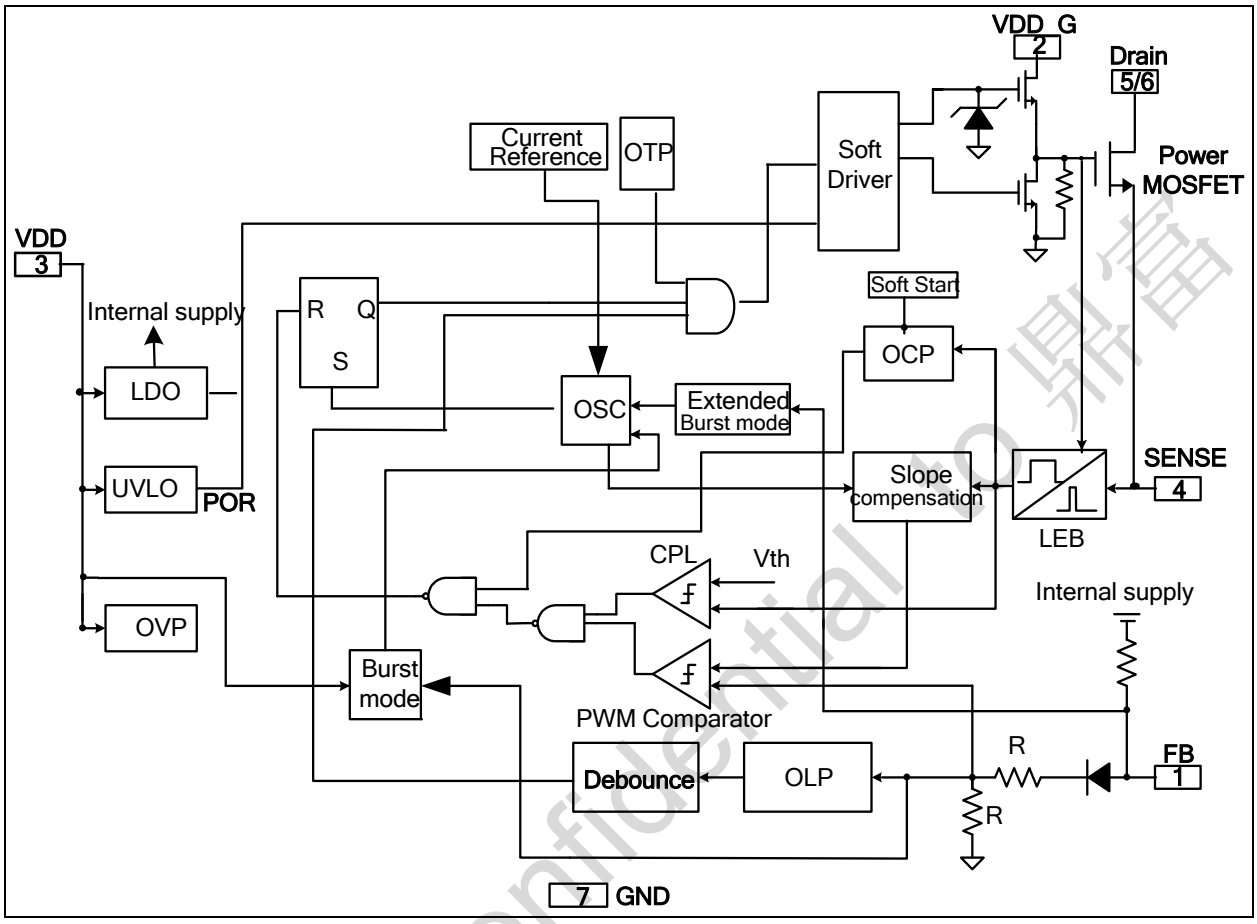
Marking Information

Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
S:DIP7 Package
P:Pb-free Package
X:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
GND	P	Ground
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4.
VDD-G	P	Internal gate driver power supply
Sense	I	Current sense input
VDD	P	IC DC power supply Input
Drain	O	HV MOSFET drain pin. The drain pin is connected to the primary lead of the transformer

BLOCK DIAGRAM



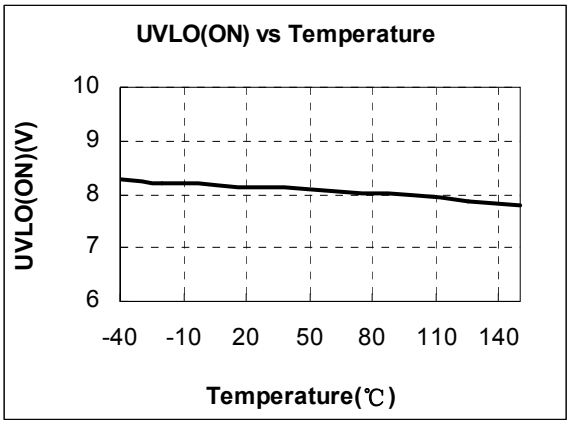
ELECTRICAL CHARACTERISTICS

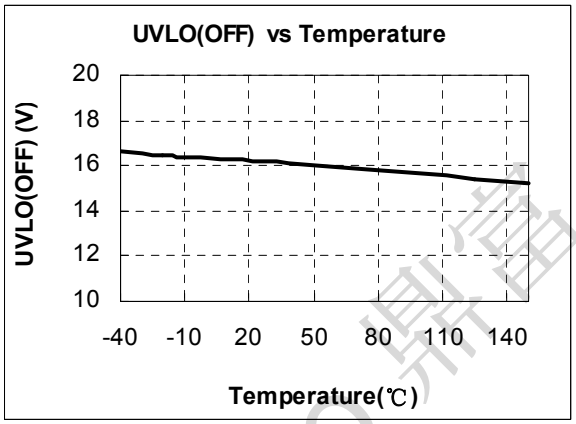
(T_A = 25℃, VDD=16V, unless otherwise noted)

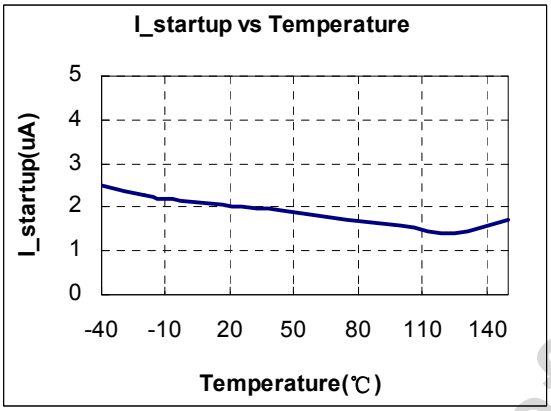
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD)						
$I_{startup}$	VDD start up current	VDD=UVLO(OFF)-1V, measure leakage current into VDD		5	20	uA
$I_{VDD\_Operation}$	Operation current	V_{FB}=3V		1.6		mA
UVLO(ON)	VDD under voltage lockout enter		7.0	8.0	9.0	V
UVLO(OFF)	VDD under voltage Lockout Exit (Recovery)		15.2	16.2	17.2	V
OVP(ON)	Over voltage protection voltage	CS=0V,FB=3V ramp up VDD until gate clock is off	27.5	29	30.5	V
Feedback input section(FB pin)						
V_{FB_OPEN}	V_{FB} Open Loop Voltage		4.9	5.5	6.1	V
I_{FB_SHORT}	FB pin short circuit current	Short FB pin to GND and measure current		0.35		mA
V_{TH_0D}	Zero duty cycle FB threshold voltage			0.8		V
V_{TH_PL}	Power limiting FB threshold voltage			4.6		V
T_{D_PL}	Power limiting debounce time			50		mSec
Z_{FB_IN}	Input impedance			15.7		Kohm
Current sense input(Sense pin)						
Soft start time				4		ms
$T_{blanking}$	Leading edge blanking time			270		ns
Z_{SENSE_IN}	Input impedance			40		Kohm
T_{D_OC}	Over current detection and control delay	From over current occurs till the gate driver output start to turn off		80		nSec
V_{TH_OC}	Internal current limiting threshold voltage	FB=3.3V	0.72	0.75	0.78	V
Oscillator						
F_{OSC}	Normal oscillation frequency		60	65	70	KHZ
$\triangle f_{Temp}$	Frequency temperature stability			5		%
$\triangle f_{VDD}$	Frequency voltage stability			5		%
D_{max}	Maximum duty cycle	FB=3.3V, CS =0V	65	75	85	%
F_{Burst}	Burst mode base frequency			22		KHZ
Mosfet section						
BVdss	MOSFET drain-source breakdown voltage		600			V
Rdson	Static drain to source on resistance			2.2		Ω
Frequency shuffling						
Δf_{OSC}	Frequency modulation range /base frequency		-4		4	%
Over temperature protection						
Over temperature protection trip point				150		℃

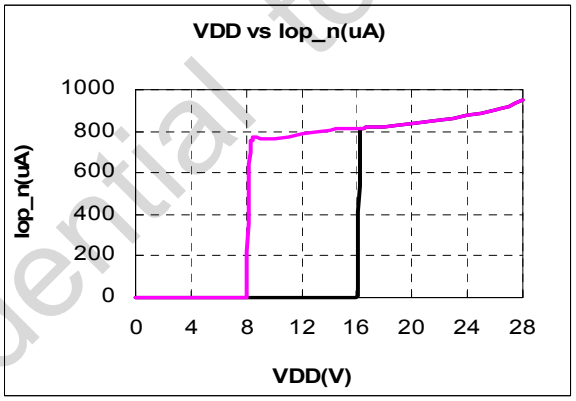
CHARACTERIZATION PLOTS

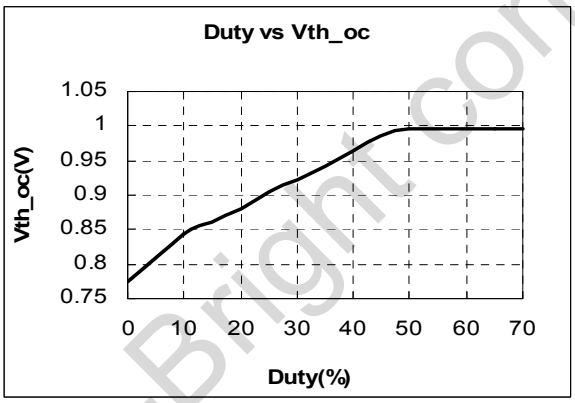
(The characteristic graphs are normalized at Ta=25℃)

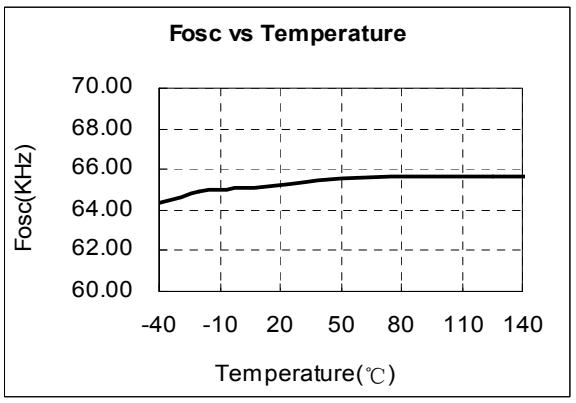


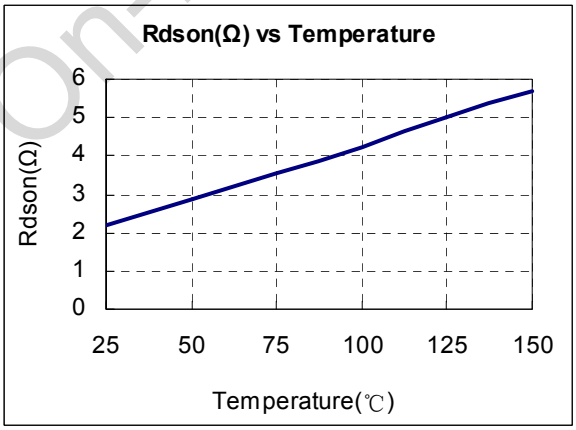












OPERATION DESCRIPTION

The OB233F is a low power off-line SMPS switcher optimized for off-line flyback converter applications. The 'extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

- **Startup current and start up control**

Startup current of OB233F is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application. For AC/DC adapter with universal input range design, startup resistors could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

- **Operating current**

The operating current of OB233F is low at 1.6mA (typical). Good efficiency is achieved with OB233F low operating current together with the 'extended burst mode' control features.

- **Soft start**

OB233F features an internal 4ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the peak current is gradually increased from nearly zero to the maximum level of 0.75V. Every restart up is followed by a soft start.

- **Frequency shuffling for EMI improvement**

The frequency shuffling (switching frequency modulation) is implemented in OB233F. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

- **Extended burst mode operation**

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss in the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.
The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below burst mode threshold level and device enters Burst Mode control. The gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.
The switching frequency control also eliminates the audio noise at any loading conditions.

- **Oscillator operation**

The switching frequency of OB233F is internally fixed at 65kHz (typical). No external frequency setting components are required for PCB design simplification.

- **Current sensing and leading edge blanking**

Cycle-by-Cycle current limiting is offered in OB233F current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of internal power MOSFET so that the external RC filtering on sense input is no longer needed. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Internal synchronized slope compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Driver**

The internal power MOSFET in OB233F is driven by a dedicated gate driver for power switch control. A too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive results in the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

In addition to the gate drive control scheme mentioned, the gate drive strength can also be adjusted externally by a resistor connected between VDD and VDDG, the falling edge of the Drain output can be well controlled. It provides great flexibility for system EMI design.

- **Protection controls**

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), over voltage protection and under voltage lockout on VDD (UVLO).

With On-Bright Proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

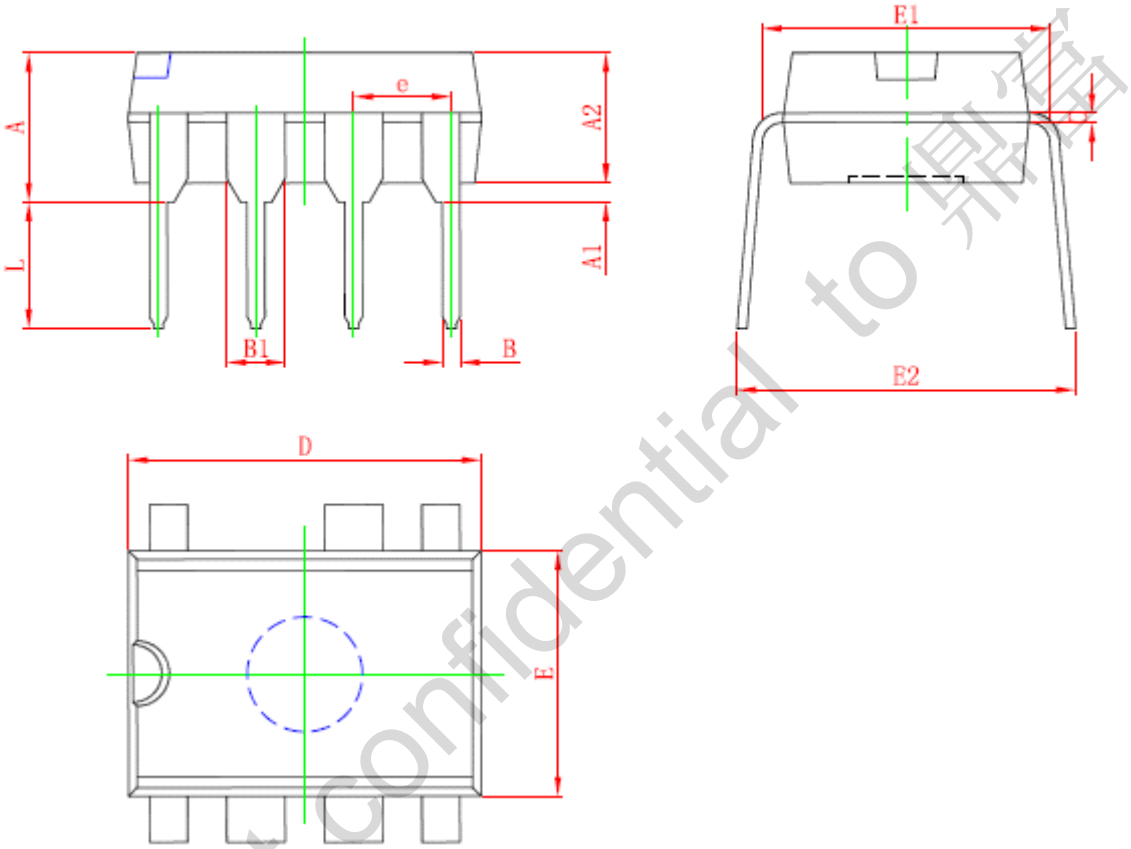
At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the switcher. Switcher restarts when VDD voltage drops below UVLO limit. Similarly, control circuit shutdowns the power MOSFET when an over temperature condition is detected or the sense pin is opened

VDD is supplied by transformer auxiliary winding output. When VDD voltage exceeds the internal OVP threshold voltage (29V, typical) due to abnormal conditions, The power MOSFET is shut down until VDD drops below 8V (typical) , and device enters power on restart-up sequence thereafter.

When the secondary rectifier is shorted, the transformer acts like a leakage inductance. Meanwhile, the current spike is extremely high. During high line input, the current in power MOSFET is too high to wait for OLP delay time. To offer reliable design, OB233F shuts down the switch and enters auto-recovery mode in this case.

PACKAGE MECHANICAL DATA

DIP7 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	2.921	4.953	0.115	0.195
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.096	7.112	0.240	0.280
E1	7.320	8.255	0.288	0.325
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	7.620	10.920	0.300	0.430

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